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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,905	08/12/2004	Chien-Jung Hsin	DROP0001USA	4904

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EXAMINER	
MEMULA, SURESH	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,905	HSIN ET AL.	
	Examiner	Art Unit	
	Suresh Memula	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/5/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. In Claim 1, lines 8-10, the terms "but" and "according" render the claim indefinite, because "but" results in the claim being incomplete, and "according" fails to distinctly identify the relationship between "first interface corresponding to the ASIC" and "updated description instruction".

4. Claims 2-17 are rejected for their dependency on rejected base Claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-8 and 10-14 are rejected under 35 U.S.C. 102(b)** as being anticipated by US Pub. No. 2002/0069396 to Bhattacharya et al. (Bhattacharya).

7. As to Claim 1,

a second interface for displaying a plurality of description instructions (Paragraph 0103) corresponding to an ASIC (Paragraph 0015) according to a variety of display instructions (Paragraphs 0094, 0103);

a first interface for inputting the display instructions (Paragraphs 0094, 0103) and for updating the description instructions (Paragraphs 0020, 0082, 0103) displayed on the second interface according to the display instructions (Paragraphs 0094, 0103); and

a logic unit (Paragraphs 0095-0096) for updating any description instruction (Paragraphs 0020, 0082, 0103) but an updated description updated by the first interface (Paragraphs 0082, 0094, 0103) corresponding to the ASIC according to the updated description instruction (Paragraphs 0020, 0060, 0082, 0094, 0099, 0103).

8. As to Claim 2, wherein the plurality of description instructions comprises a timing slack report of the ASIC (Paragraphs 0021, 0032, 0052, 0060, 0073, 0103).

9. As to Claim 3, wherein the plurality of description instructions comprises a netlist of the ASIC (Paragraphs 0020, 0060, 0082).

10. As to Claim 4, wherein the plurality of description instructions comprises a noise analysis report of the ASIC (Paragraphs 0034, 0070, 0103).

11. As to Claim 5, wherein the plurality of description instructions comprises a power analysis report of the ASIC (Paragraphs 0009, 0033, 0052, 0103).

12. As to Claim 6, wherein the logic unit is further capable of calculating a noise analysis report (Paragraphs 0034, 0070, 0103) corresponding to an updated netlist (Paragraph 0082).

13. As to Claim 7, wherein the logic unit is further capable of calculating a power analysis report (Paragraphs 0009, 0033, 0052, 0103) corresponding to an updated netlist (Paragraph 0082).

14. As to Claim 8, wherein the logic unit is further capable of calculating a timing slack report (Paragraphs 0021, 0032, 0052, 0060, 0073, 0103) corresponding to an updated netlist (Paragraph 0082).

15. As to Claim 10, wherein the logic unit is further capable of executing a timing optimization process (Paragraphs 0021, 0089, 0096).

16. As to Claim 11, wherein the logic unit is further capable of executing a cell & wire extraction process (Paragraphs 0056, 0061-0062) and for generating a cell & wire delay (Paragraphs 0061, 0076) of a SDF (Paragraph 0094).

17. As to Claim 12, wherein the second interface (Paragraph 0103) is capable of displaying cells and interconnects connected between the cells of the ASIC (Abstract; Paragraphs 0007-0008, 0012, 0032; FIG. 3, 7) according to a specified display instruction input to the first interface (Abstract; Paragraphs 0060, 0094, 0099, 0103).

18. As to Claim 13, wherein the second interface is capable of further displaying spare cells neighboring the cells (Paragraph 0092) according to the specified display instruction (Abstract; Paragraphs 0060, 0094, 0099, 0103).

19. As to Claim 14, wherein the second interface is capable of displaying a plurality of specified icons (Abstract; Paragraph 0103; FIG. 3, 7), each of the icons corresponding to a specified cell having a specified function corresponding to the specified icon (Abstract; Paragraph 0103; FIG. 3, 7).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claim 9 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Bhattacharya in view of one or more of: US Pub. No. 2005/0015738 to Alpert et al. (Alpert), US Pub. No. 2005/0102643 to Hou et al. (Hou), and/or US Pub. No. 2004/0243957 to Mandry (Mandry).

22. Bhattacharya teaches substantially all of the limitations as stated above, except for clock tree synthesis.

23. Alpert discloses clock tree synthesis (Paragraph 0026), Hou discloses clock tree synthesis (Paragraph 0019), and Mandry discloses clock tree synthesis (Paragraph 0065).

24. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized clock tree synthesis; as taught by Alpert (Paragraph 0026), Hou (Paragraph 0019), and/or Mandry (Paragraph 0065); in order to synthesize a gate array logic circuit to allow optimal topological arrangement of the gate array on the logic circuit (Hou: Paragraph 0019), since methods/tools for clock tree synthesis are conventional (Alpert: Paragraph 0026) and typical (Mandry: Paragraph 0065).

25. **Claims 15-17 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Bhattacharya in view of one or more of: US Patent No. 6,209,122 to Jyu et al. (Jyu), US Patent No. 6,425,110 to Hathaway et al. (Hathaway '110), US Pub. No. 2005/0246117 to Hathaway et al. (Hathaway '117), and/or US Patent No. 7,089,143 to Foreman et al. (Foreman).

26. Bhattacharya teaches substantially all of the limitations as stated above, except for timing slack sub-reports.

27. Jyu discloses timing slack sub-reports (Column 11, lines 50-60), Hathaway '110 discloses timing slack sub-reports (Column 11, lines 30-31), Hathaway '117 discloses timing slack sub-reports (Paragraph 0050), and Foreman discloses timing slack sub-reports (Column 8, lines 62-67).

28. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized timing slack sub-reports; as taught by Jyu (Column 11, lines 50-60), Hathaway '110 (Column 11, lines 30-31), Hathaway '117 (Paragraph 0050), and/or Foreman (Column 8, lines 62-67); in order to account for timing requirements at each clock-controlled device (Jyu: Column 11, lines 50-60), produce separate slack values at many internal points in a design (Hathaway '110: Column 11, lines 30-31), determine slack values for each element in an integrated circuit (Hathaway '117: Paragraph 0050), and/or provide an additive result of individual clocks or data signals of interest (Foreman: Column 8, lines 62-67).

29. Pursuant to Claim 16, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to circuit components referenced by the timing slack report (Hathaway '117: Paragraph 0050).

30. Pursuant to Claim 17, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to clocks referenced by the timing slack report (Jyu: Column 11, lines 50-60; Foreman: Column 8, lines 62-67).

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suresh Memula
Art Unit 2825
December 13, 2006

PAUL DINH
PRIMARY EXAMINER